

10

10

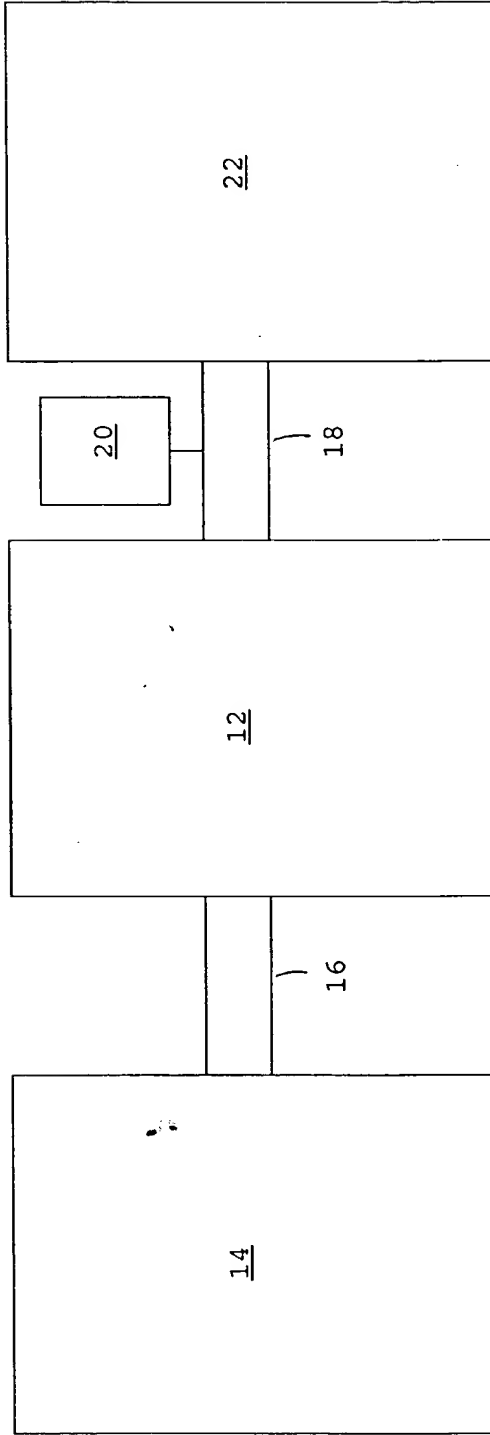


FIG. 1

FIG. 2

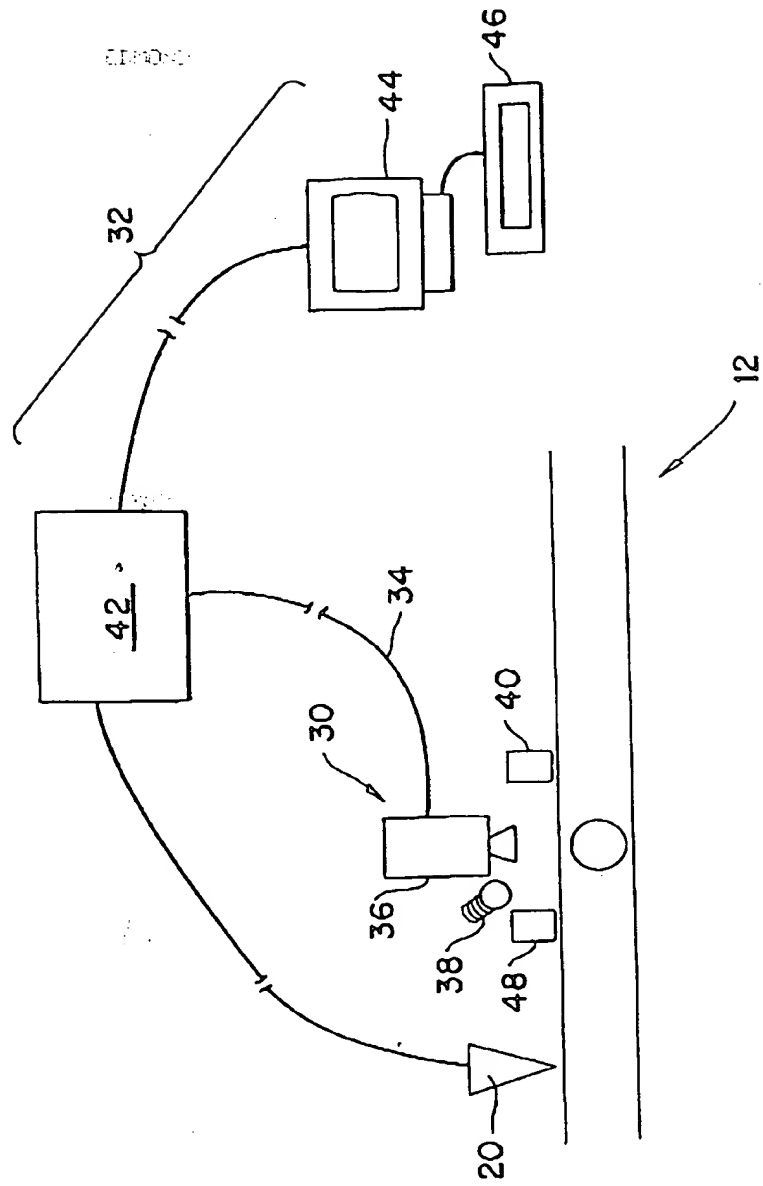


FIG. 3 is a block diagram of a system 50, including a first unit 10, a second unit 10, a third unit 10, and a fourth unit 10. The first unit 10 is connected to the second unit 10 via a first connection 52. The second unit 10 is connected to the third unit 10 via a second connection 52. The third unit 10 is connected to the fourth unit 10 via a third connection 52. The first unit 10 is also connected to a first input/output port 12. The second unit 10 is also connected to a second input/output port 12. The third unit 10 is also connected to a third input/output port 12. The fourth unit 10 is also connected to a fourth input/output port 12.

50

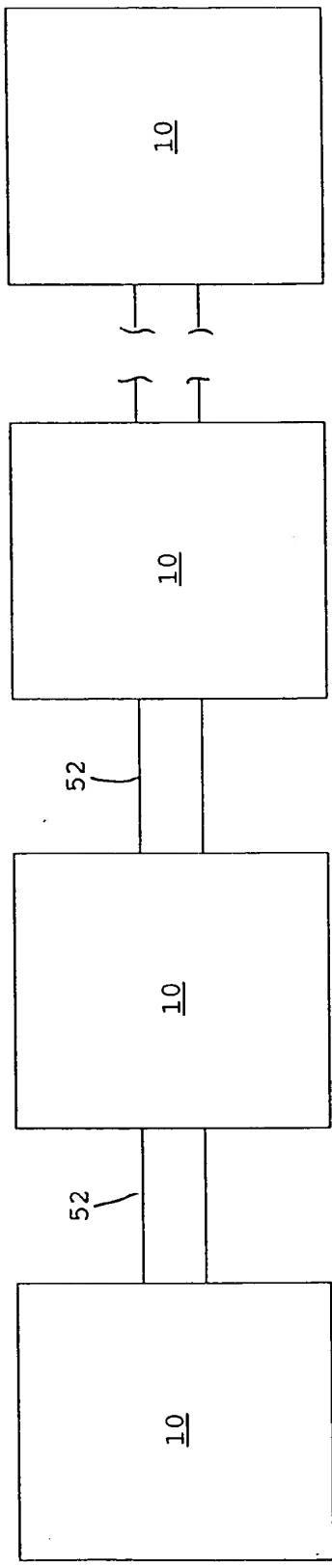
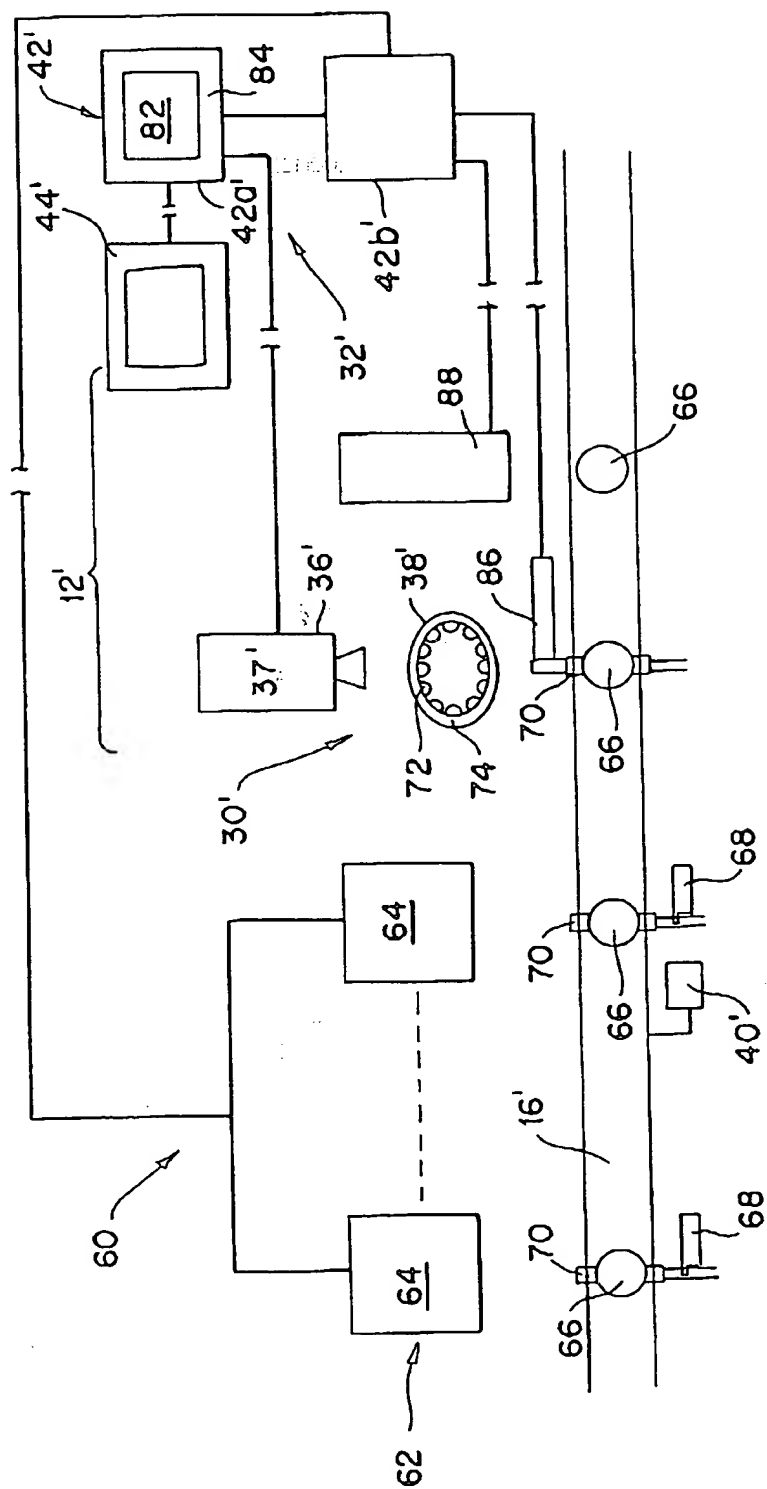


FIG. 3



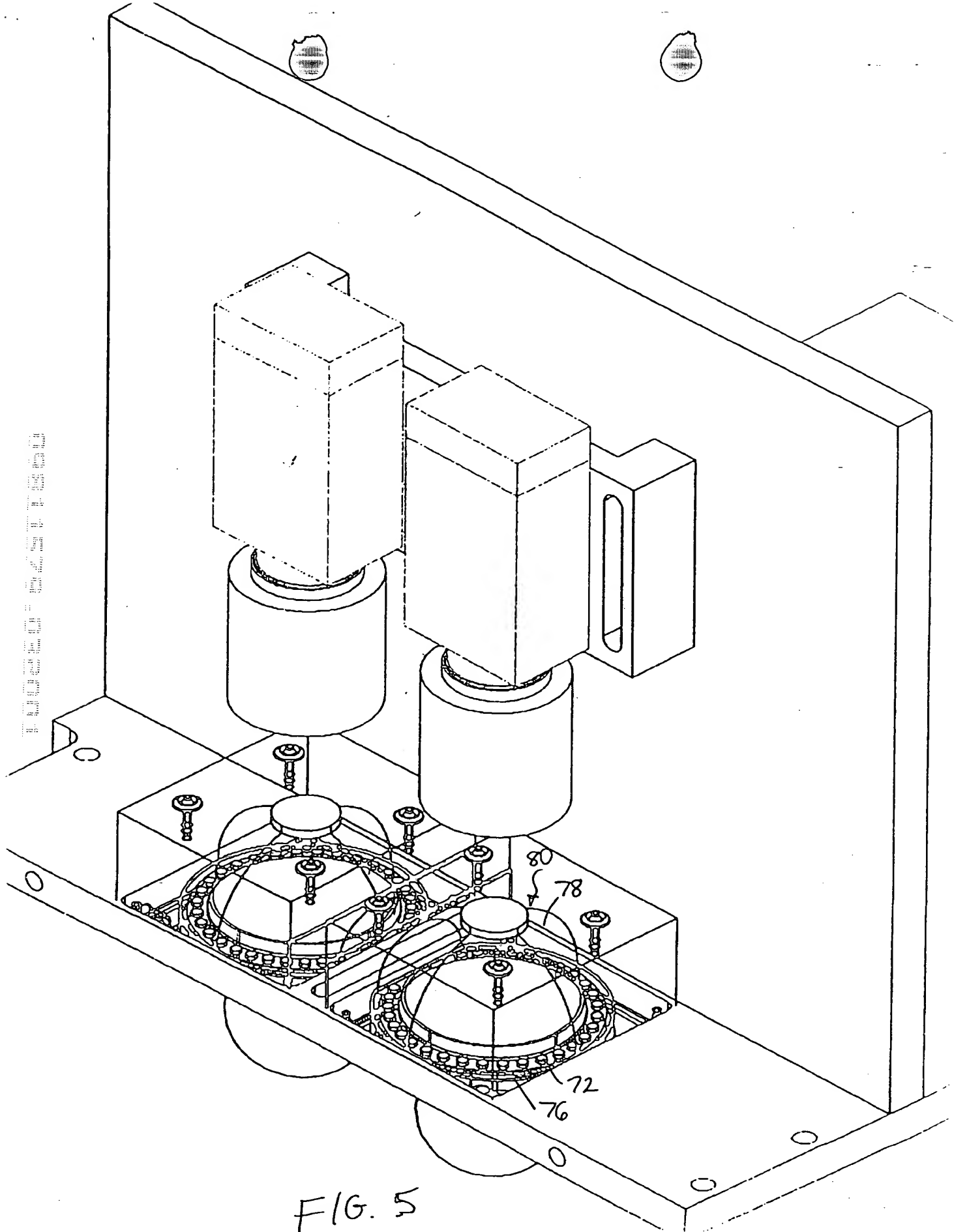


FIG. 5

FIG. 6

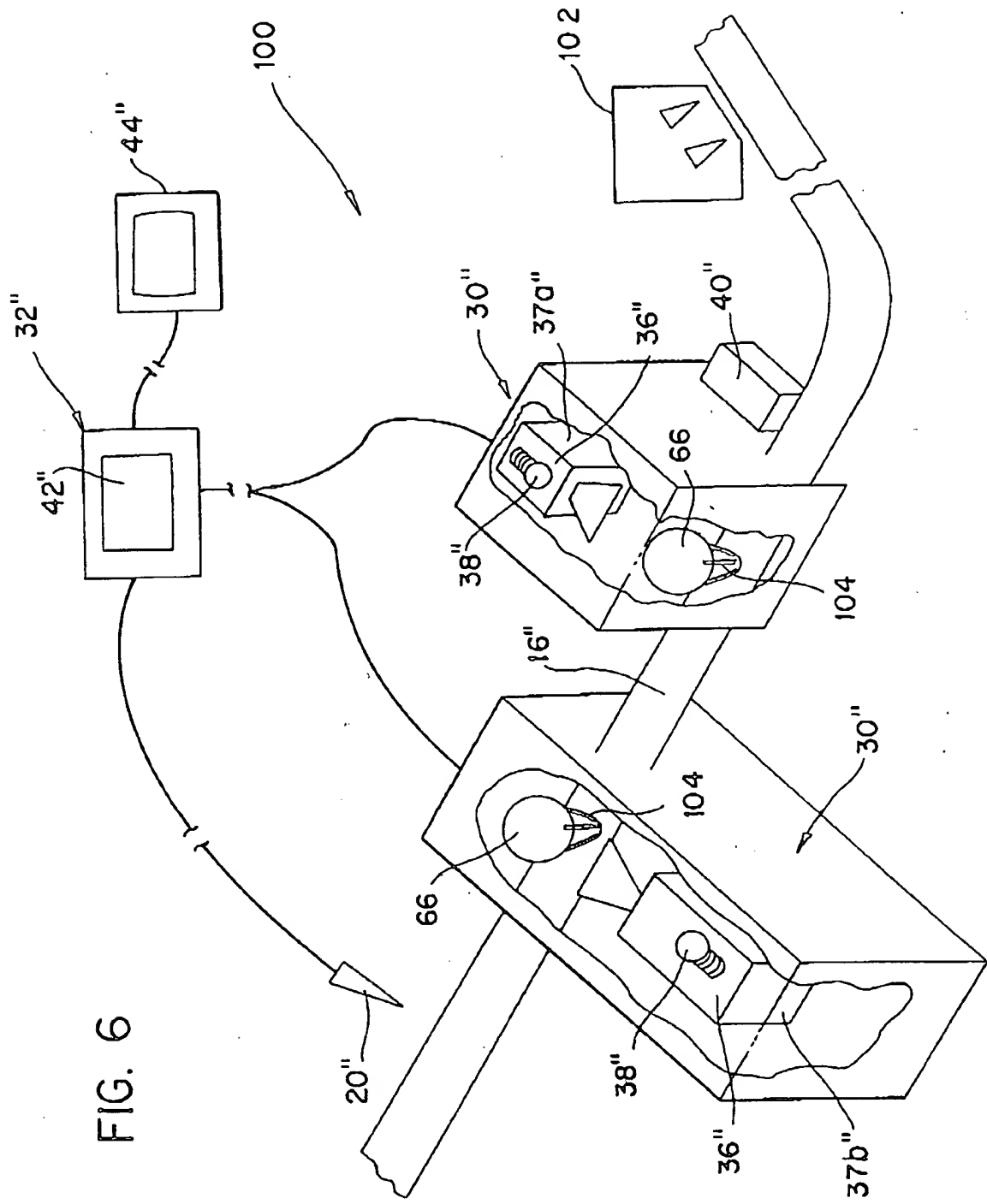


FIG. 7 is a block diagram of a system 120. The system 120 includes a processor 124, a memory 126, and a network interface 122. The processor 124 is connected to the memory 126 and the network interface 122. The memory 126 is connected to the network interface 122. The network interface 122 is connected to a network 128.

120

128

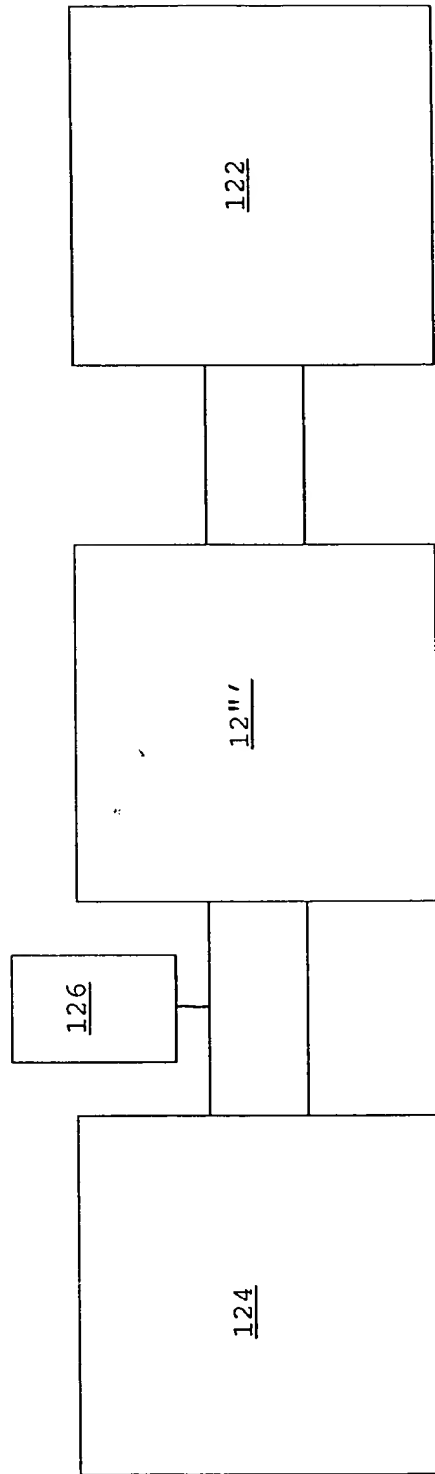


FIG. 7